

FORM PTO-1449				Atty. Docket No. XA-9485A		Appln. No.	
<u>LIST OF DOCUMENTS CITED BY APPLICANT</u>							
				Applicant Masaya MURANAKA et al.			
				Filing Date HEREWITH		Group	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
TB	AA	6,560,725 B1	05/2003	Longwell et al.	714	54	
	AB	6,065,146 A	05/2000	Bosshart, Patrick	714	754	
	AC	6,236,602 B1	05/2001	Patti, Robert	365	201	
	AD	4,794,597 A	12/1988	Ooba et al.	714	703	
	AE	4,758,992 A	07/1988	Taguchi, Masao	365	222	
	AF						
	AG						
	AH						
	AI						
FOREIGN PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
TB	AJ	11-213659	08/06/99	Japan			Abstract
	AK	07-262794	10/13/95	Japan			Abstract
	AL	11-007760 A	01/12/99	Japan			Abstract
	AM						
	AN						
	AO						
OTHER (including author, title, date, pertinent pages, etc.)							
TB	AP	Mano, T.; Yamada, J.; Inoue, J.; Nakajima, S.; Circuit Techniques For A VLSI Memory, IEEE Journal of Solid-State Circuits, Volume: 18 Issue: 5, October 1983, Pages 463-470					
	AQ						
	AR						
Examiner /Timothy Bonura/				Date Considered 10/05/2006			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							